CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20Vp-p can be achieved by digital signal amplitudes of 4.5V to 20V (if V_{DD}-V_{SS} = 3V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0V, and V_{EE} = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic “1” is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the “CHANNEL IN/OUT” terminals are the outputs and the “COMMON OUT/IN” terminals are the inputs.

Features

- Wide Range of Digital and Analog Signal Levels
  - Digital ............................................ 3V to 20V
  - Analog ............................................ \( \leq 20\text{V}_{p-p} \)
- Low ON Resistance, 125\( \Omega \) (Typ) Over 15\( \text{V}_{p-p} \) Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of \( \pm 100\mu\text{A} \) (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to 20\( \text{V}_{p-p} \) (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, \( r_{ON} = 5\Omega \) (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2\( \mu\text{W} \) (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1\( \mu\text{A} \) at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4051BF, CD4052BF, CD4053BF</td>
<td>-55 to 125</td>
<td>16 Ld CERAMIC DIP</td>
</tr>
<tr>
<td>CD4051BE, CD4052BE, CD4053BE</td>
<td>-55 to 125</td>
<td>16 Ld PDIP</td>
</tr>
<tr>
<td>CD4051BM, CD4051BNS</td>
<td>-55 to 125</td>
<td>16 Ld SOIC</td>
</tr>
<tr>
<td>CD4051BPW, CD4052BPW, CD4053BPW</td>
<td>-55 to 125</td>
<td>16 Ld TSSOP</td>
</tr>
</tbody>
</table>
**Pinouts**

CD4051B (PDIP, CDIP, SOIC, TSSOP)

**TOP VIEW**

<table>
<thead>
<tr>
<th>CHANNLES IN/OUT</th>
<th>4</th>
<th>1</th>
<th>10</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>COM OUT/IN</td>
<td>6</td>
<td>2</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>CHANNELS IN/OUT</td>
<td>7</td>
<td>4</td>
<td>13</td>
<td>0</td>
</tr>
<tr>
<td>INH</td>
<td>5</td>
<td>5</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>VEE</td>
<td>11</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>10</td>
<td>B</td>
<td></td>
<td>9</td>
</tr>
</tbody>
</table>

CD4052B (PDIP, CDIP, TSSOP)

**TOP VIEW**

<table>
<thead>
<tr>
<th>CHANNLES OUT/IN</th>
<th>0</th>
<th>1</th>
<th>15</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMMON &quot;Y&quot; OUT/IN</td>
<td>2</td>
<td>2</td>
<td>14</td>
<td>1</td>
</tr>
<tr>
<td>CHANNELS IN/OUT</td>
<td>3</td>
<td>4</td>
<td>13</td>
<td>0</td>
</tr>
<tr>
<td>INH</td>
<td>1</td>
<td>5</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>VEE</td>
<td>6</td>
<td>6</td>
<td>11</td>
<td>1</td>
</tr>
<tr>
<td>VSS</td>
<td>7</td>
<td>7</td>
<td>10</td>
<td>A</td>
</tr>
</tbody>
</table>

CD4053B (PDIP, CDIP, TSSOP)

**TOP VIEW**

<table>
<thead>
<tr>
<th>CHANNEL IN/OUT</th>
<th>16</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN/OUT by bx</td>
<td>15</td>
<td>OUT/IN bx OR by</td>
</tr>
<tr>
<td>OUT/IN cy</td>
<td>14</td>
<td>OUT/IN ax OR ay</td>
</tr>
<tr>
<td>OUT/IN CX</td>
<td>13</td>
<td>ay</td>
</tr>
<tr>
<td>IN/OUT CX</td>
<td>12</td>
<td>ax</td>
</tr>
<tr>
<td>INH</td>
<td>11</td>
<td>A</td>
</tr>
<tr>
<td>VEE</td>
<td>10</td>
<td>B</td>
</tr>
<tr>
<td>VSS</td>
<td>9</td>
<td>C</td>
</tr>
</tbody>
</table>

**Functional Block Diagrams**

**CD4051B**

- Logic Level Conversion
- Binary to 1 of 8 Decoder with Inhibit

All inputs are protected by standard CMOS protection network.
Functional Block Diagrams (Continued)

CD4052B

CD4053B

† All inputs are protected by standard CMOS protection network.
### TRUTH TABLES

<table>
<thead>
<tr>
<th>INPUT STATES</th>
<th>“ON” CHANNEL(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INHIBIT</td>
<td>C</td>
</tr>
<tr>
<td>CD4051B</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
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<tr>
<td></td>
<td>0</td>
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<td></td>
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<td></td>
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</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>CD4052B</td>
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<td></td>
<td>0</td>
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<td></td>
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<tr>
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<td></td>
<td>1</td>
</tr>
<tr>
<td>CD4053B</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

X = Don’t Care
### Absolute Maximum Ratings

**Supply Voltage (V+ to V−)**
- Voltages Referenced to VSS Terminal: -0.5V to 20V
- DC Input Voltage Range: -0.5V to VDD +0.5V
- DC Input Current, Any One Input: ≤10mA

**Operating Conditions**
- Temperature Range: -55°C to 125°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. The package thermal impedance is calculated in accordance with JESD51.

### Electrical Specifications

#### Common Conditions Here: If Whole Table is For the Full Temp. Range, V_SUPPLY = ±5V, A_V = +1,
- R_L = 100Ω, Unless Otherwise Specified (Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LIMITS AT INDICATED TEMPERATURES (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIGNAL INPUTS (V_IS) AND OUTPUTS (V_OS)</td>
<td>V_IS (V)</td>
<td>V_EE (V)</td>
</tr>
<tr>
<td>Quiescent Device Current, I_DD Max</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Drain to Source ON Resistance r_ON Max</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Change in ON Resistance (Between Any Two Channels), Δr_ON</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Capacitance: Input, C_IS</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output, C_OS</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>CD4051</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>CD4052</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>CD4053</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Feedthrough C_IOS</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Propagation Delay Time (Signal Input to Output)</td>
<td>V_DD</td>
<td>R_L = 200kΩ, C_L = 50pF, t_{r}, t_{f} = 20ns</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>-</td>
</tr>
</tbody>
</table>
### Electrical Specifications

**CD4051B, CD4052B, CD4053B**

#### Common Conditions Here: If Whole Table is For the Full Temp. Range, $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $RL = 100\Omega$, Unless Otherwise Specified (Continued) (Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LIMITS AT INDICATED TEMPERATURES (°C)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{IS}$ (V)</td>
<td>$V_{EE}$ (V)</td>
<td>$V_{SS}$ (V)</td>
</tr>
<tr>
<td><strong>CONTROL (ADDRESS OR INHIBIT), $V_C$</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage, $V_{IL}$, Max</td>
<td>$V_{IL} = V_{DD}$ through $1k\Omega$; $V_{IL} = V_{DD}$ through $1k\Omega$</td>
<td>$V_{EE} = V_{SS}$, $RL = 1k\Omega$ to $V_{SS}$, $I_{IS} &lt; 2\mu A$ on All OFF Channels</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>Input High Voltage, $V_{IH}$, Min</td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>Input Current, $I_{IN}$ (Max)</td>
<td>$V_{IN} = 0$, $18 V_{OS}$</td>
<td>$\pm 0.1$</td>
<td>$\pm 0.1$</td>
</tr>
<tr>
<td>Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figures 10, 11, 14</td>
<td>$t_r$, $t_f = 20$ns, $C_L = 50pF$, $R_L = 10k\Omega$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-5</td>
<td>0</td>
</tr>
<tr>
<td>Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning ON) See Figure 11</td>
<td>$t_r$, $t_f = 20$ns, $C_L = 50pF$, $R_L = 1k\Omega$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10</td>
<td>0</td>
</tr>
<tr>
<td>Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning OFF) See Figure 15</td>
<td>$t_r$, $t_f = 20$ns, $C_L = 50pF$, $R_L = 10k\Omega$</td>
<td>0</td>
<td>0</td>
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<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10</td>
<td>0</td>
</tr>
<tr>
<td>Input Capacitance, $C_{IN}$ (Any Address or Inhibit Input)</td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**NOTE:**

2. Determined by minimum feasible leakage measurement for automatic testing.

### Electrical Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{IS}$ (V)</td>
<td>$V_{DD}$ (V)</td>
<td>$RL$ (kΩ)</td>
</tr>
<tr>
<td>Cutoff (-3dB) Frequency Channel ON (Sine Wave Input)</td>
<td>$V_{OS}$ at Common OUT/IN</td>
<td>CD4053</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>$V_{EE} = V_{SS}$, $V_{OS} = \pm 3dB$</td>
<td>CD4052</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>$20\log \frac{V_{OS}}{V_{IS}}$</td>
<td>CD4051</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CD4053</td>
<td>60</td>
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**Electrical Specifications**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
<th>TYP</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Total Harmonic Distortion, THD</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 (Note 3)</td>
<td>5</td>
<td>10</td>
<td>0.3</td>
<td>%</td>
</tr>
<tr>
<td>3 (Note 3)</td>
<td>10</td>
<td></td>
<td>0.2</td>
<td>%</td>
</tr>
<tr>
<td>5 (Note 3)</td>
<td>15</td>
<td></td>
<td>0.12</td>
<td>%</td>
</tr>
<tr>
<td>$V_{EE} = V_{SS}, f_{IS} = 1kHz$ Sine Wave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-40dB Feedthrough Frequency (All Channels OFF)</td>
<td>5 (Note 3)</td>
<td>10</td>
<td>1</td>
<td>$V_{OS}$ at Common OUT/IN</td>
</tr>
<tr>
<td>$V_{EE} = V_{SS}$</td>
<td></td>
<td>$20 \log \frac{V_{OS}}{V_{IS}} = -40$ dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-40dB Signal Crosstalk Frequency</td>
<td>5 (Note 3)</td>
<td>10</td>
<td>1</td>
<td>Between Any 2 Channels</td>
</tr>
<tr>
<td>$V_{EE} = V_{SS}$</td>
<td></td>
<td>$20 \log \frac{V_{OS}}{V_{IS}} = -40$ dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address-or-Inhibit-to-Signal Crosstalk</td>
<td>-</td>
<td>10</td>
<td>10 (Note 4)</td>
<td>$V_{DD} - V_{EE}$</td>
</tr>
<tr>
<td>$V_{EE} = 0, V_{SS} = 0, t_r, t_f = 20ns, V_{CC} = V_{DD} - V_{EE}$ (Square Wave)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
3. Peak-to-Peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$
4. Both ends of channel.

**Typical Performance Curves**

![FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)](image1)

![FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)](image2)
**Typical Performance Curves (Continued)**

**FIGURE 3. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)**

**FIGURE 4. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)**

**FIGURE 5. ON CHARACTERISTICS FOR 1 OF 8 CHANNELS (CD4051B)**

**FIGURE 6. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4051B)**

**FIGURE 7. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4052B)**

**FIGURE 8. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4053B)**
**Test Circuits and Waveforms**

**FIGURE 9. TYPICAL BIAS VOLTAGES**

NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = VSS and "1" = VDD. The analog signal (through the TG) may swing from VEE to VDD.

**FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON**

(RL = 1kΩ)

**FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF**

(RL = 1kΩ)

**FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF**
Test Circuits and Waveforms (Continued)

FIGURE 13. OFF CHANNEL LEAKAGE CURRENT - ALL CHANNELS OFF

FIGURE 14. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT

FIGURE 15. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT

FIGURE 16. INPUT VOLTAGE TEST CIRCUITS (NOISE IMMUNITY)
Test Circuits and Waveforms (Continued)

**FIGURE 17. QUIESCENT DEVICE CURRENT**

**FIGURE 18. CHANNEL ON RESISTANCE MEASUREMENT CIRCUIT**

**FIGURE 19. INPUT CURRENT**

**FIGURE 20. FEEDTHROUGH (ALL TYPES)**

**FIGURE 21. CROSSTALK BETWEEN ANY TWO CHANNELS (ALL TYPES)**

**FIGURE 22. CROSSTALK BETWEEN DUALS OR TRIPLETS (CD4052B, CD4053B)**
**Special Considerations**

In applications where separate power sources are used to drive V<sub>DD</sub> and the signal inputs, the V<sub>DD</sub> current capability should exceed V<sub>DD</sub>/R<sub>L</sub> (R<sub>L</sub> = effective external load). This provision avoids permanent current flow or clamp action on the V<sub>DD</sub> supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.
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